AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A compensation module for ~~the~~ phase compensation of clock signals~~, in particular a compensation module for~~ in a telecommunications network ~~or for a network device of a telecommunications network~~, comprising receiving means for receiving ~~at least one~~ first and second clock signal and a second clock signal, wherein the compensation module comprises: ~~comprising~~

first delay means for delaying the ~~at least one~~ first clock signal by a first delay time to obtain a delayed first clock signal,

second delay means for delaying the second clock signal by a second delay time to obtain a delayed second clock signal, and

adjusting means for the phase adjustment of the second delay means, so that the delayed~~,~~ second clock signal~~, present at the output end of the second delay means,~~ is adapted to the phase of the delayed~~, at least one~~ first clock signal ~~present at the~~ output end of the first delay means.

2. (currently amended): A compensation module according to Claim 1, wherein at least one of the first delay time and~~/or~~ a start value for the second delay time are predetermined as at least one of:

a function of a maximum expected phase difference between the at least one first clock signal and the second clock signal, and

~~and/or as~~ a function of a maximum expected propagation time difference which is caused by transmission paths of different length used for the transmission of the at least one first clock signal and the second clock signal, respectively.

3. (currently amended): A compensation module according to Claim 1, wherein the first delay means are designed ~~such that they~~ to delay the at least one first clock signal by at least a first delay time, which ~~is such that it~~ corresponds to at least one of a maximum expected phase difference and/~~or~~ a maximum expected propagation time difference between the at least one first clock signal and the second clock signal and, wherein the propagation time ~~which~~ difference is caused by transmission paths of different length used for the transmission of the at least one first clock signal and the second clock signal, respectively.

4. (currently amended): A compensation module according to Claim 1, wherein the second delay means are designed ~~such that they~~ to delay the at least one second clock signal by at least a second delay time, which ~~is such that it~~ corresponds to at least one of twice a maximum expected phase difference and/~~or~~ twice a maximum expected propagation time difference between the at least one first clock signal and the second clock signal, ~~which~~ and wherein the propagation time difference is caused by transmission paths of different length used for the transmission of the at least one first clock signal and the second clock signal, respectively.

5. (currently amended): A compensation module according to Claim 1, further comprising selection means for selecting one of the at least one first delayed clock signal and ~~or~~

the second delayed clock signal and,~~/or~~ optionally, one of the at least one first clock signal ~~or~~ and the second clock signal, where the respective selected, at least one first delayed clock signal or second delayed clock signal and~~/or~~ the at least one first clock signal or second clock signal serves ~~in particular~~ to synchronise the compensation module.

6. (currently amended): A compensation module according to Claim 5, wherein the selection means are designed to select, for a delay in the first delay means, ~~that~~ one of the at least one first clock signal or second clock signal, which is identified by an item of master-slave-status information as a master synchronisation signal or which leads in phase the respective other first or second clock signal ~~in phase~~.

7. (original): A compensation module according to Claim 5, wherein the selection means are designed to select the at least one first delayed clock signal or the second delayed clock signal while the compensation module is in operation.

8. (currently amended): A compensation module according to Claim 1, wherein the adjusting means are designed to adjust the phase of the first delay means, and wherein, ~~so that in particular~~ when the first delayed clock signal is selected instead of the second delayed clock signal, the delayed first clock signal, present at ~~the~~ an output end of the first delay means, is adapted, by said adjusting means, to the phase of the delayed second clock signal present at ~~the~~ an output end of the second delay means.

9. (currently amended): A compensation module according to Claim 1, wherein the adjusting means are designed to preferentially adjust at least one of the first delay time and/~~or~~ the second delay time to a first or second start value, respectively, which ~~is~~ are either predetermined ~~and/~~or ~~is~~ determined upon each start-up of the compensation module, wherein, ~~where~~ a modification of the first delay time or the second delay time, which increases ~~the~~ a deviation of the first delay time or second delay time from the first start value or the second start value, respectively, is performed only upon ~~the attainment~~ attaining ~~of~~ a predetermined first deviation tolerance value, while the converse applies upon ~~the attainment of~~ attaining a second deviation tolerance value which is smaller than the first deviation tolerance value.

10. (currently amended): A compensation module according to Claim 1, wherein the adjusting means are designed ~~such that,~~ for the phase adjustment, ~~they~~ and wherein the adjusting means changes the second delay time in a stepped fashion.

11. (currently amended): A compensation module according to Claim 1, wherein the adjusting means are designed ~~such that,~~ for the phase adjustment, and wherein the adjusting means ~~they~~ changes the second delay time of the second delay means in dynamic step sizes, ~~the~~ a respective step size being modified as a function of a respective phase difference between the delayed second clock signal, present at the output end of the second delay means, and the delayed first clock signal present at the output end of the first delay means.

12. (currently amended): A compensation module according to Claim 1, wherein the first delay means, the second delay means, and the adjusting means comprise~~ing~~ a program code ~~which can be~~ executed by a control means of a network device~~, in particular a control means on a console of a network device for a transmission network with a synchronous digital hierarchy~~.

13. (currently amended): A computer-readable medium storing program code executed by a control means of a network device, the program code comprising:

a receiving module receiving at least one first clock signal and a second clock signal;

a first delay module delaying the at least one first clock signal by a first delay time;

a second delay module delaying the second clock signal by a second delay time; and

an adjustment module adjusting a phase of the second delay module,

wherein the delayed, second clock signal is adapted to a phase of the delayed, at least one first clock signal.

~~memory means, in particular a floppy disc, CD-ROM, digital versatile disc, hard disc drive or the like, with a compensation module according to Claim 12 stored thereon.~~

14. (currently amended): A network device~~, in particular a network device~~ for a transmission network with a synchronous digital hierarchy, the network device comprising a compensation module for a phase compensation of clock signals in the network with the synchronous digital hierarchy, wherein the compensation module comprises:

receiving means for receiving at least one first clock signal and a second clock signal,

first delay means for delaying the at least one first clock signal by a first delay time,

second delay means for delaying the second clock signal by a second delay time, and

adjusting means for a phase adjustment of the second delay means, where the delayed second clock signal is adapted to a phase of the delayed at least one first clock signal~~, with at least one compensation module according to Claim 1~~.

15. (currently amended): A method of phase compensation between at least one first clock signal and a second clock signal which are transmitted to ~~a compensation module, in particular~~ a compensation module in a telecommunications network or in a network device of ~~a~~ the telecommunications network, the method comprising ~~the steps of~~:

receiving the at least one first clock signal and the second clock signal;

delaying by the compensation module the at least one first clock signal, by a predetermined first delay time to form a delayed first clock signal;~~,~~

delaying by the compensation module the second clock signal by a predetermined second delay time to form a delayed second clock signal, and

modifying by the compensation module the second delay time such that the delayed second clock signal is adapted to the phase of the delayed, at least one first clock signal.

16. (new): The compensation module according to claim 1, wherein the network device further comprises output means outputting two clock signals.

17. (new): The compensation module according to claim 1, wherein the first and second clock signals are external clock signals received over the telecommunications network.

18. (new): The compensation module according to Claim 1, wherein the compensation module comprises program code executed by a control means on a console of a network device for a transmission network with a synchronous digital hierarchy.

19. (new): The compensation module according to claim 1, wherein the delayed first clock signal and the delayed second clock signal are frame clock signals and wherein the second clock signal is redundant to the first clock signal.

20. (new): The method of phase compensation according to claim 15, wherein the delayed second clock signal, which is present at an output of a second delay module delaying the second signal, is adapted to the phase of the delayed at least one first clock signal, that is present at an output of a first delay module delaying the at least one first clock signal, and wherein the second clock signal is redundant to the first clock signal.